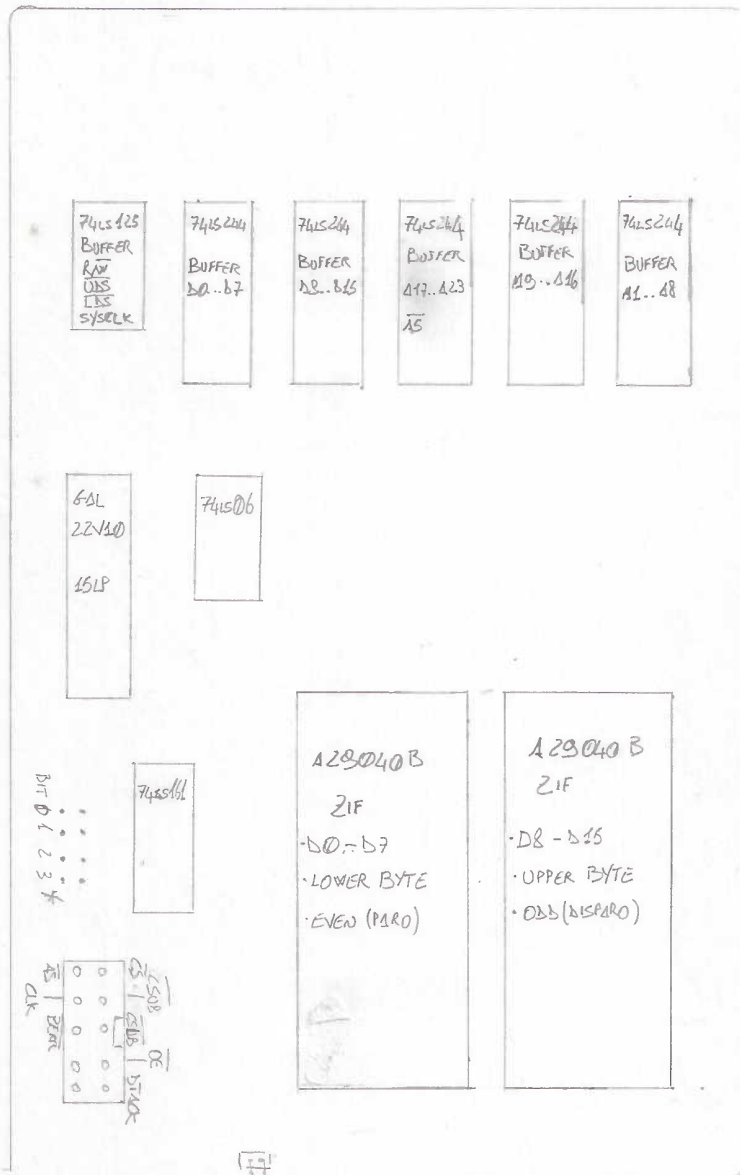
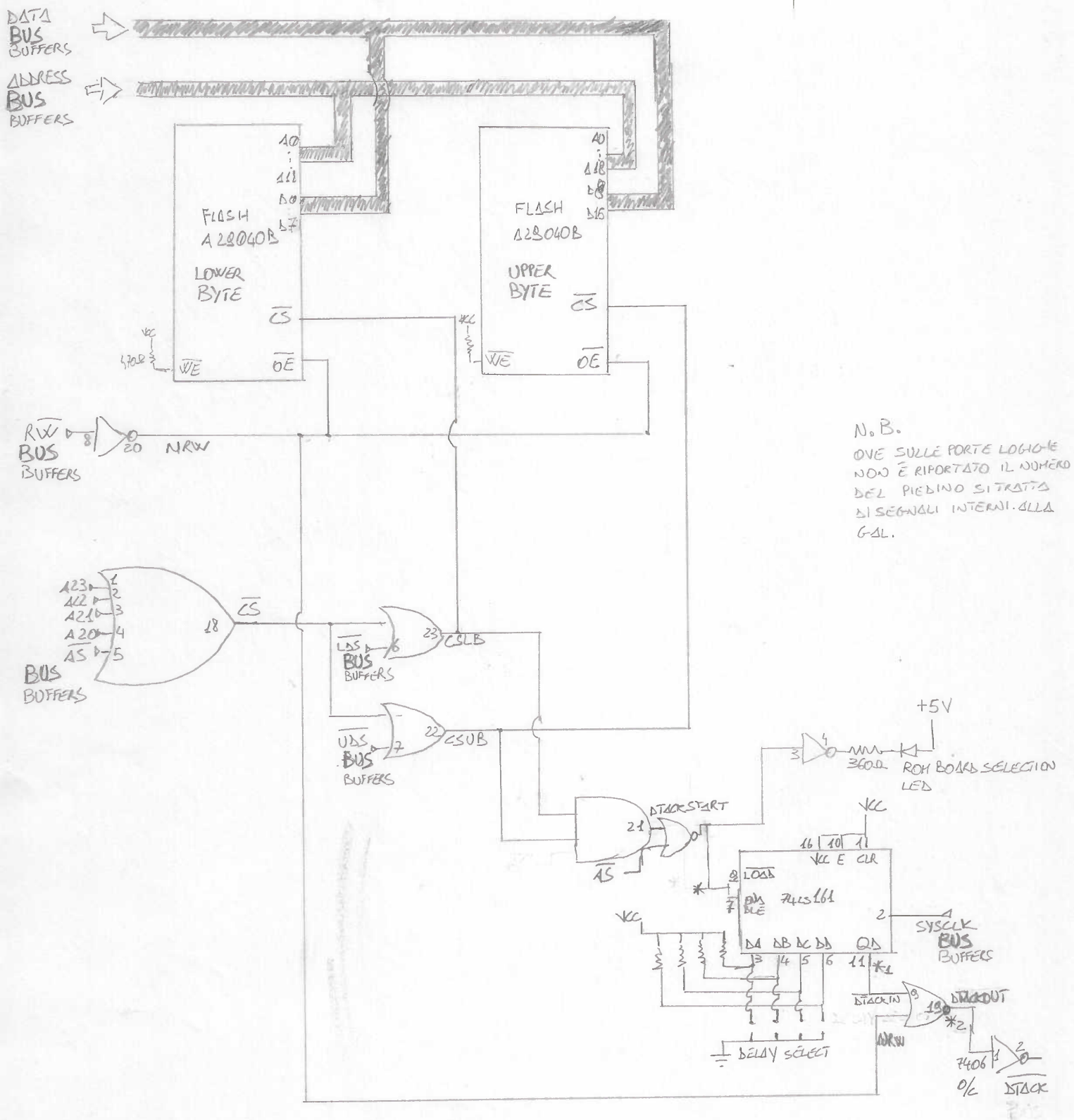


ROM BOARD DISPOSIZIONE COMPONENTI



* TUTTO APERTO MINIMO RITARDO

ROM BOARD



N.B.
 OVE SULLE PORTE LOGICHE
 NON È RIPORTATO IL NUMERO
 DEL PIEDINO SI TRATTA
 DI SEGNALI INTERNI ALLA
 GAL.

* IL COLLEGIO DEL 161 PER INSERIRE I CICLI DI RITARDO
 PARTE CON STACKSTART ALTO.

*₁ QD VA BASSO QUANDO GLI N CICLI DI RITARDO SI SONO COMPIUTI.
 (STACK IN)

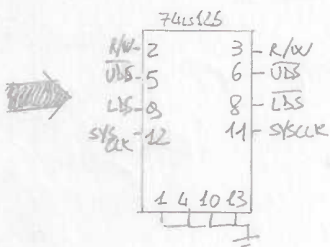
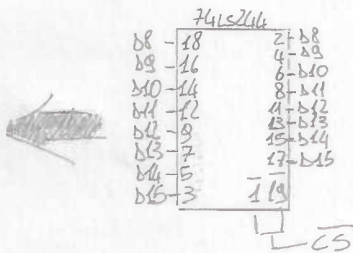
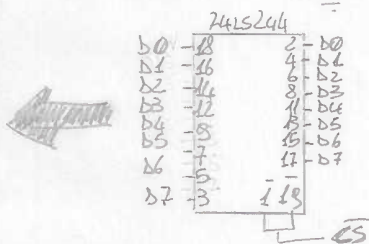
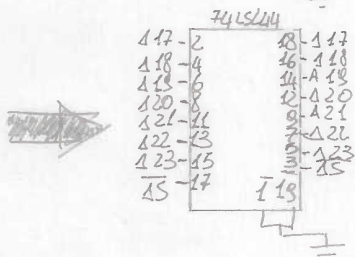
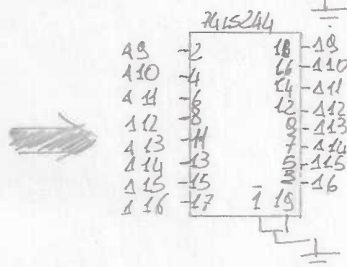
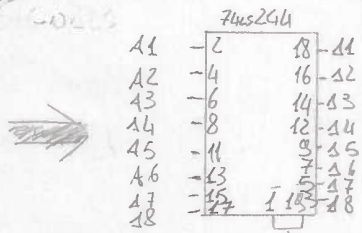
*₂ STACK OUT VA ALTO SE RW È ALTO (NRW BASSO) E SE STACK IN È BASSO.

IL CONTROLLO SU RW (NRW) VIENE ESEGUITO PER NON ASSERIRE STACK AL PROCESSORE QUANDO SI TENTA DI SCRIVERE IN ROM.

ROM BOARD BUFFERING

SIGNALS FROM - TO
BUS

SIGNALS TO - FROM
ROM BOARD



PIN	ROW A	ROW B	ROW C
1	D00	BBSY* V/A	D08
2	D01	BCLR* V/A	D09
3	D02	ACFAIL*E	D10
4	D03	BG0IN* BR	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN* BG	D13
7	D06	BG1OUT* NO	D14
8	D07	BG2IN* BG	D15
9	GND	BG2OUT*	GND
10	SYSCLK CLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1* UBS	BR0* IACK1	SYSRESET* IACK1
13	DS0* UBS	BR1* IACK2	LWORD*
14	WRITE* R/W	BR2* IACK3	AM5 FC2
15	GND	BR3* IACK4	A23
16	DTACK*	AM0 IACK5	A22
17	GND	AM1 IACK6	A21
18	AS*	AM2 IACK7	A20
19	GND	AM3 FC0	A19
20	IACK*	GND	A18
21	IACKIN	SERCLK	A17
22	IACKOUT* 200	SERDAT	A16
23	AM4 FC1	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

ANALISI ROM BOARD CIRCUITO STACK

Listing<1>

File Window Edit Options Markers Invasm Help

Group Run

Markers

G1 Time 5.215 us from Trigger

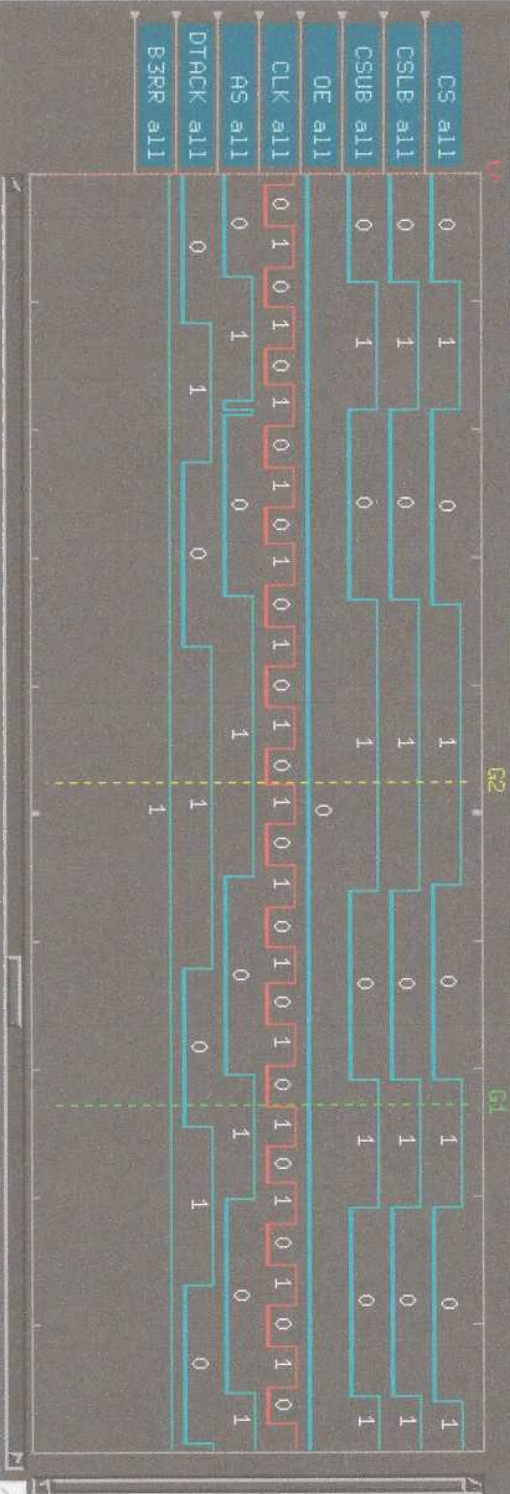
State Number	ADDR	68010 Mnemonic	DATA	STAT
Decimal	Hex	hex	Hex	Binary
-10	11FEF6	1BFE unknown (000) write (6800)	1BFE	10000000
-9	004086	1BFE unknown (000) write (6800)	1BFE	10000000
-8	1044B6	1BFE unknown (000) write (6800)	1BFE	10000000
-7	114200	1BFE unknown (000) write (6800)	1BFE	10000000
-6	0076B6	1BFF unknown (000) write (6800)	1BFF	10000000
-5	00FEA6	1BFF unknown (000) write (6800)	1BFF	10000000
-4	000000	ORI,B #00,D0	0000	11101001
-3	000002	0000 supr program read	0000	11101001
-2	000004	ORI,B #00,D0	0000	11101001
-1	000006	0400 supr program read	0400	11101001
0	000400	MOVEA,L #000000AC,A0	207C	11101001
1	000402	0000 supr program read	0000	11101001
2	000404	00AC supr program read	00AC	11101001
3	000406	MOVEA,L #00000005,D0	203C	11101001
4	000408	0000 supr program read	0000	11101001
5	00040A	0005 supr program read	0005	11101001
6	00040C	NOP	4E71	11101001
7	00040E	DBEQ D0,00040C	57C8	11101001
8	000410	FFFC supr program read	FFFC	11101001
G1 9	00040C	NOP	4E71	11101001
10	00040E	DBEQ D0,00040C	57C8	11101001
11	000410	FFFC supr program read	FFFC	11101001
12	00040C	NOP	4E71	11101001
13	00040E	DBEQ D0,00040C	57C8	11101001
14	000410	FFFC supr program read	FFFC	11101001
15	00040C	NOP	4E71	11101001
16	00040E	DBEQ D0,00040C	57C8	11101001
17	000410	FFFC supr program read	FFFC	11101001
18	00040C	NOP	4E71	11101001
19	00040E	DBEQ D0,00040C	57C8	11101001

ESECUZIONE ISTRUZIONE NOP

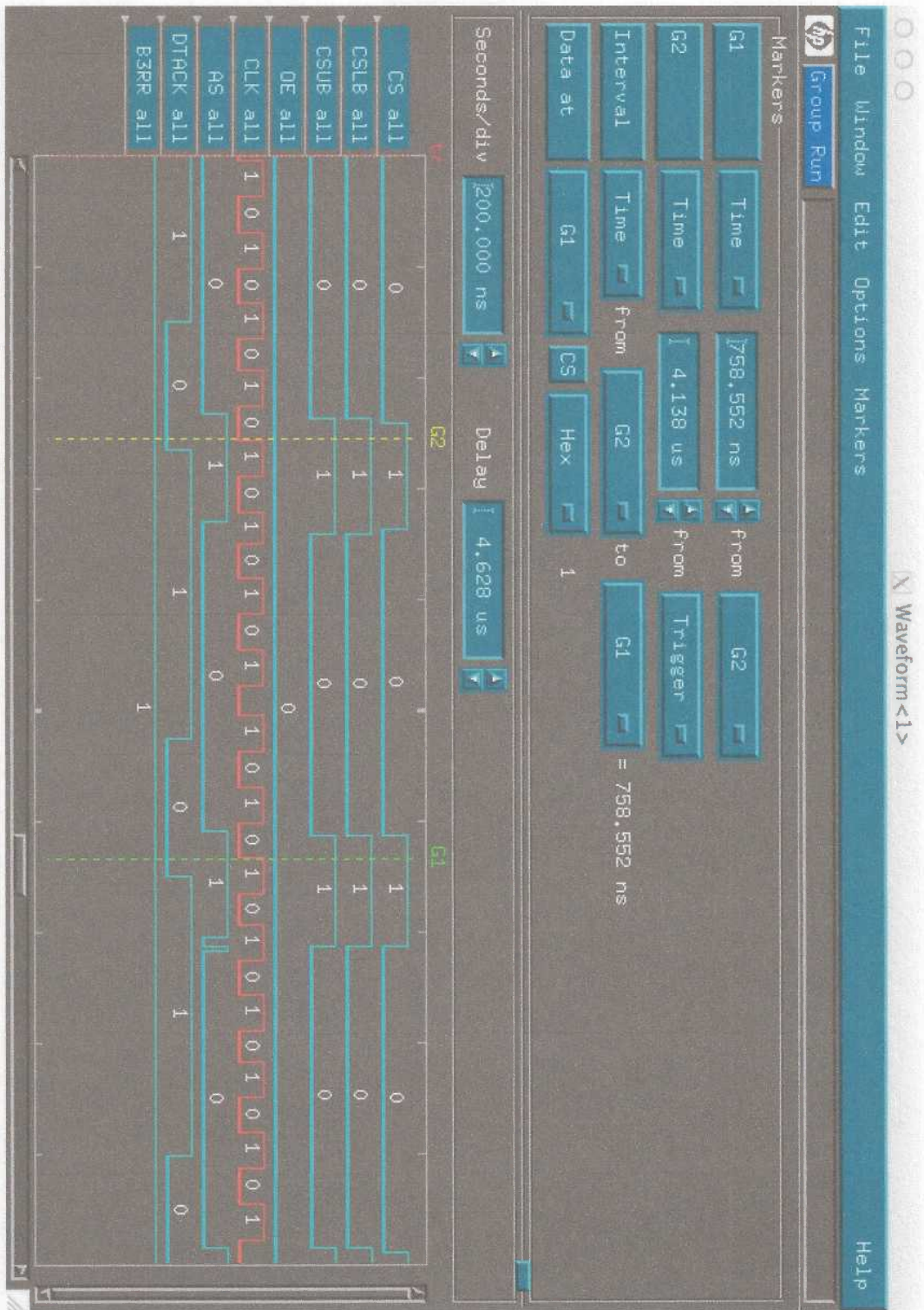
Markers

G1	Time	507.041 ns	From	G2		
G2	Time	4.644 us	From	Trigger		
Interval	Time	from	G2	to	G1	= 507.041 ns
Data at	G1	CS	Hex	1		

Seconds/div 200.000 ns Delay 4.692 us



SEV8A R1T4R1 S0 DTACK



CON RTARDI SU DTACK.
 SUMER SU BIT DE 1 SULLA ROH BOARD